Fardeen Rahman

Email: fardeen.mm.rahman@gmail.com fardeenrahman.com Mobile: 0444-559-904

EDUCATION

Adelaide University

Adelaide, SA

Bachelor of Science in Computer Science — GPA: 6.10/7.00

March. 2024 - Present

Glenunga International High School

ATAR of 97.80/99.95

Glenunga, SA Feb. 2018 - Dec. 2023

EXPERIENCE

Australian Institute of Machine Learning

Adelaide, SA

FPGA Research Assistant Internship Nov. 2025 - Present

• LiteX: Used LiteX to test and create FPGA Cores/System-on-Chips to explore various digital design architectures and create full FPGA-based systems.

- RISC-V Strucutre: RISC-V is an open standard instruction architecture that I researched and tested under the supervision of Dr Bradley Morgan. We explored the acceleration of this platform's hardware using quantum resilient algorithms, also known as quantum cryptography.
- Kyber ISE: Designed and implemented a unique CPU core, using the LiteX framework and HDL (Verilog/VHDL), integrating an open-source RISC-V core and developing a memory-mapped bus structure. Eventually, I integrated custom hardware acceleration blocks to test.

Realty1Global

Adelaide, SA

Full Stack Developer

Aug 2025 - Present

o Next.js with React and API integration: Developed a full-stack short-term rental platform using Next.js, React, and Tailwind CSS, implementing secure booking workflows and integrating Stripe for end-to-end payment processing.

Volunteering

Adelaide University Computer Science Club

Adelaide, SA

Social Media and Design Officer

Oct. 2025 - Present

Open Source Team

Oct. 2024 - Oct. 2025

Adelaide University Space Society

Adelaide, SA

Marketing and Design Officer Open Source Manager

Nov. 2025 - Present

Nov. 2025 - Present

Awards and Achievements

Jane Street Estimathon Winner

Adelaide, SA

Won in a group of five

Sept. 2024

• Winner: Employed several techniques, such as Fermi Estimation and logical reasoning, to achieve the highest point total of the pool of competitors.

Adelaide University Principals Scholarship

Adelaide, SA

Recommended for academic excellence

March. 2024

Projects

- Basys 2 VGA Controller: Engineered and implemented a custom 640x480 VGA Controller and Pong entirely within the Basys 2 FPGA (Spartan-3E), demonstrating high-speed digital system design. Designed critical clock division and synchronization logic to derive the necessary pixel clock and generate precise Horizontal and Vertical Sync (HSync/VSync) signals required for the 60 Hz video standard.
- fardeenrahman.com: My personal portfolio website developed using Astro, Tailwind CSS and Typescript. Integrated content management system for easy modular editing over my career. Deployed using Vercel.
- Adelaide University Space Society Website: Developed an open-source website in Vercel with Next. is and React, with end-to-end Stripe payment integration. Used calendar library with React to show event schedules as well as a content management system so admin members do not have to hard-code changes.

Programming Skills

- Languages: Verilog, VHDL, Python, Javascript, C++, C, SQL, Typescript, Astro, HTML, Java, Assembly
- Technologies: Physical FPGAs, LiteX, AWS, React, Vue, Google API